REMARKS/ARGUMENTS

This paper responds to the Office Action of March 25, 2004. Applicant respectfully requests reconsideration of the application. The shortened statutory period runs through June 25, 2004. Accordingly, this response is timely.

Claims 1-72 are now pending, a total of 72 claims. Claims 1, 2, 9, 32, 39, 57 and 61 are independent.

I. Preliminary Amendment

A Preliminary Amendment were submitted February 20, 2001. However, the Preliminary Amendment has not been acknowledged. For the Examiner's convenience and ready reference, a replacement copy of the February 2001 Preliminary Amendment is enclosed herewith. I certify that this Preliminary Amendment was deposited with the United States Postal Service on February 20, 2001 as First Class Mail in an envelope with sufficient postage addressed to The Commissioner for Patents, Washington D.C. 20231, and is entitled to entry as of that date, pursuant to 37 C.F.R. § 1.8. Applicant requests confirmation that this Preliminary Amendment is entered.

II. Claims 1, 2, 9, 32, 39, 57 and 61

The Office Action discusses claims 1, 2, 9, 32, 39, 57 and 61 in connection with the Blomgren '009 and Blomgren '750 patents. Claim 2 recites as follows:

> 2. A method, comprising the steps of:
>
> decoding instructions of a user-state program coded in a RISC instruction set in a hardware instruction decoder of a computer, the RISC instruction set being an instruction set having fixed-length instructions and a load/store/operate organization; and
>
> decoding instructions of a user-state program coded in a CISC instruction set in a CISC hardware instruction decoder of a computer, the CISC instruction set being an instruction set having variable-length instructions and many instructions having multiple side-effects; and
>
> the instructions decoded by the CISC decoder and RISC decoder being executed in a common execution pipeline;

> a RISC instruction set of the RISC decoder designed to share a substantial portion of its opcode values with corresponding opcodes of the CISC instruction set.

The last paragraph of claim 2 is supported, for example, by Fig. 9C and at page 163. Fig. 9C shows that, at least for a substantial number of instructions, the opcodes are identical between the X86 CISC instruction set and the RISC instruction set. Applicants were the first to recognize that a RISC instruction set could be designed with significant correspondences to a CISC instruction set. This recognition may have benefits in certain embodiments. For example, such a RISC instruction set can serve dual purposes: (a) it can be used by assembly language programmers to program the machine, and (b) it can easily be used as the microcode instruction set for implementation of the CISC instruction set, with a very simple instruction decoder.[1]

The Blomgren '009 and '750 designers did not recognize the value of this correspondence, or make any attempt to design it into their system. Instead, Blomgren tries to combine two instruction sets, the Intel X86 and IBM PowerPC, that were not designed to have any particular correspondence to each other. If there are any correspondences at all, they are purely accidental, not the product of "design" as recited in claim 2. Compare for example, the opcode map for the PowerPC (Blomgren '750, table 2, at col. 11-12) with the opcode map for the X86 (Blomgren '750, table 3 at col. 13-14). Blomgren '750 shows that Intel defines ADD instructions with opcodes 0000000, 00000001, 00000010, 00000011, 00000100, and 00000101. The PowerPC opcode map shows ADD instructions with opcodes 001100, 001101, 001110, 001111. There is no correspondence reflected in this design.

Because Blomgren '009 and '750 do not show "a RISC instruction set ... having a substantial portion of its opcodes defined to correspond to corresponding opcodes of the CISC instruction set," any rejection may be withdrawn.

Claims 1, 9, 32, 39, 57 and 61 are patentable for similar reasons.

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[1] Equivalents to the amended limitations may exist. As one example, a simple one-to-one mapping between the CISC opcodes and the RISC opcodes might be equivalent in some circumstances. Other equivalents to other limitations may exist.

III. Dependent claims

The dependent claims recite further limitations that further patentably distinguish the art. They are patentable with the independent claims discussed above, and further for reasons recited in these claims.

For example, claims 4 and 14 recite an "an intra-instruction program counter." This corresponds to the "FRAC" bits 931/932 of Fig. 9A, discussed at pages 170-71 of the specification. These bits provide a "fractional" intra-instruction program counter that measures partial progress of an instruction. This permits tracking partial completion of an instruction, so that an interrupted instruction may be restarted from its intermediate completion point, rather than restarted from its beginning. In contrast, Blomgren '009 at col. 14, lines 22-34 teaches a "SRR0" register that always "points to the CISC instruction" next to be executed. Blomgren never suggests that SRR0 can assume an intra-instruction "fractional" value to indicate that a partially-completed CISC instruction should be restarted at some intra-instruction midpoint.

IV. Conclusion

In view of the amendments and remarks, Applicant respectfully submits that the claims are in condition for allowance. Applicant requests that the application be passed to issue in due course. The Examiner is urged to telephone Applicant's undersigned counsel at the number noted below if it will advance the prosecution of this application, or with any suggestion to resolve any condition that would impede allowance. In the event that any extension of time is required, Applicant petitions for that extension of time required to make this response timely.

Kindly charge any additional fee, or credit any surplus, to Deposit Account No. 23-2405, Order No. 114596-26-0051BS.

Respectfully submitted,

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By: _____

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